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10/661,535	09/15/2003	Hitoshi Hirakawa	122.1568	8025

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EXAMINER	
SHERMAN, STEPHEN G	

ART UNIT	PAPER NUMBER
2674	

DATE MAILED: 02/08/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/661,535	HIRAKAWA ET AL.	
	Examiner	Art Unit	
	Stephen G. Sherman	2674	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 September 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. Figures 1-4 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-2, 4, 9-10 and 19-20 are rejected under 35 U.S.C. 102(b) as being anticipated by Awaji (JP 2000-148085 A).

Regarding claim 1, Awaji discloses a method for driving a plasma display panel, wherein

a display field, corresponding to a display of a screen, is composed of a plurality of subfields (Drawing 3 and Paragraph [0029]. The display field f is divided into 5 subfields sf1-sf5.),

a gradation display is realized by combining subfields to be lit among the plurality of subfields (Paragraph [0029]. The examiner interprets that since the display field is divided into subfields in order to perform a gradation display that a gradation display would be realized by the combination of these subfields.),

each subfield comprises at least an address period to write cells to be lit in the subfield and a sustain period to cause light emission to occur in the written cells (Drawing 3 and paragraphs [0029]-[0030]. In Drawing 3 it can be seen that there is an address period TA and a sustain period TS.), and

all of the cells to be lit in a display field are lit in a predetermined subfield among the plurality of subfields making up the display field (Drawing 3 and paragraph [0031]. The examiner interprets that making all of the discharge cells turn on is equivalent to lighting all of the cells.).

Regarding claim 2, Awaji discloses a method for driving a plasma display panel, as set forth in claim 1, wherein the predetermined subfield is a subfield with the lowest luminance ratio (Paragraph [0017]. The examiner interprets that the smallest subfield is the subfield with the lowest luminescence ratio.).

Regarding claim 4, Awaji discloses a method for driving a plasma display panel, as set forth in claim 1, wherein the predetermined subfield is the subfield at the head in a display field (Paragraph [0017]. The examiner interprets that since the adjustment could be made in the any subfield, that the subfield at the head would be a subfield where the adjustment could be made.).

Regarding claim 9, Awaji discloses a method for driving a plasma display panel, as set forth in claim 1, wherein the subfield with the lowest luminance ratio is arranged at the head in a display field and the predetermined subfield is arranged in the second position in the display field (Drawing 3 and paragraphs [0029]-[0032]. The examiner interprets that since the discharge occurs in sf2, that this is the subfield in the second position and that the display field at the head is the one with the lowest luminance ratio since the sustain period for that subfield is the smallest.).

Regarding claim 10, Awaji discloses a method for driving a plasma display panel, as set forth in claim 9, wherein the predetermined subfield is one with the second lowest luminance ratio (Drawing 3 and paragraph [0031]. The examiner interprets that since sf2 is in the second position and has the second smallest sustain period that it is the subfield with the second lowest luminance ratio.).

Regarding claim 19, A method for driving a plasma display panel, as set forth in claim 1, wherein the gradation display level is determined with the luminance due to lighting in the predetermined subfield being taken into consideration (Paragraph [0031]. The examiner interprets that if the predetermined subfield is sf2 which is part of the gradation display level that the predetermined subfield would be taken into consideration.).

Regarding claim 20, Awaji discloses a plasma display device comprising a plasma display panel and a driving circuit for the plasma display panel, wherein the driving circuit drives the plasma display panel using the driving methods set forth in claim 1 (Drawings 1 and 2).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

6. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Awaji (JP 2000-148085 A) in view of Naka et al. (US 2002/0191008).

Regarding claim 3, Awaji discloses a method for driving a plasma display panel, as set forth in claim 1.

Awaji fails to teach a method wherein a display field has a subfield with a same luminance ratio as that of the predetermined subfield, in addition to the predetermined subfield.

Naka et al. disclose of a method for driving a plasma display panel wherein a display field has two subfields with the same luminance ratio (Figure 12 and paragraphs [0091]-[0094]. Figure 12 shows SF3-SF6 containing the same luminance ratio.).

Therefore it would have been obvious to "one of ordinary skill" in the art at the time the invention was made to use the method of having two subfields with the same luminance ratio as taught by Naka et al. with the method of driving a plasma display panel as taught by Awaji to reduce false contour interference as a problem in moving image display based on the subfield method.

7. Claims 5-6 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Awaji (JP 2000-148085 A) in view of Tokunaga et al. (2003/0011540).

Regarding claim 5, Awaji discloses a method for driving a plasma display panel, as set forth in claim 1.

Awaji fails to teach of a method wherein an all-cell write discharge is caused to occur in the predetermined subfield before the address period.

Tokunaga et al. disclose a method for driving a plasma display panel wherein an all-cell write discharge is caused to occur in a subfield before the address period (Paragraph [0032]. The examiner interprets that initializing the cells into a lit discharge state is an all-cell write discharge and that this happens prior to the address period.).

Therefore it would have been obvious to "one of ordinary skill" in the art at the time the invention was made to use the method of having an all-cell write discharge before the address period as taught by Tokunaga et al. with the method of driving a plasma display panel as taught by Awaji in order to provide a plasma display panel drive method that produces a stable discharge effect while increasing contrast.

Regarding claim 6, Awaji discloses a method for driving a plasma display panel, as set forth in claim 1. Awaji also discloses wherein the predetermined subfield is also a subfield with a heavy weight of luminance (Paragraph [0017]. The examiner interprets that the largest subfield is the one with the heavy weight of luminance.).

Awaji fails to teach of a method wherein an all-cell write discharge is caused to occur in the predetermined subfield before the address period.

Tokunaga et al. disclose a method for driving a plasma display panel wherein an all-cell write discharge is caused to occur in a subfield before the address period (Paragraph [0032]. The examiner interprets that initializing the cells into a lit discharge state is an all-cell write discharge and that this happens prior to the address period. The examiner interprets then that if the predetermined subfield is a subfield with a heavy weight of luminance that an all-cell write discharge would be caused to occur in the predetermined subfield and a subfield with a heavy weight of luminance before the address period.).

Therefore it would have been obvious to "one of ordinary skill" in the art at the time the invention was made to use the method of having an all-cell write discharge before the address period as taught by Tokunaga et al. with the method of driving a plasma display panel as taught by Awaji in order to provide a plasma display panel drive method that produces a stable discharge effect while increasing contrast.

Regarding claim 11, Awaji discloses a method for driving a plasma display panel, as set forth in claim 9.

Awaji fails to teach a method wherein an all-cell write discharge is caused to occur in the subfield at the head and the predetermined subfield before the address period.

Tokunaga et al. disclose a method for driving a plasma display panel wherein an all-cell write discharge is caused to occur in the subfield at the head and all other subfields before the address period (Figure 2A and paragraphs [0011] and [0018]. The

examiner interprets that the full reset Rc is the all-cell write discharge, which is cause to occur in every subfield of Figure 2A, which would include the subfield at the head and the predetermined subfield.).

Therefore it would have been obvious to "one of ordinary skill" in the art at the time the invention was made to use the method of having an all-cell write discharge before the address period as taught by Tokunaga et al. with the method of driving a plasma display panel as taught by Awaji in order to provide a plasma display panel drive method that produces a stable discharge effect while increasing contrast.

8. Claims 7-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Awaji (JP 2000-148085 A) in view of Tokunaga et al. (2003/0011540) and further in view of Tokunaga et al. (US 2003/0067425).

Regarding claim 7, Awaji and Tokunaga et al. (2003/0011540) disclose a method for driving a plasma display panel, as set forth in claim 5.

Awaji and Tokunaga et al. (2003/0011540) fail to teach a method wherein the all-cell write discharge is caused to occur twice successively in the predetermined subfield.

Tokunaga et al. (US 2003/0067425) disclose a method for driving a plasma display panel wherein a reset is caused to occur twice in a subfield (Figure 18 and paragraph [0158]. R_{ODD} and R_{EVE} are both reset charges which are each caused to occur in a single subfield.).

Therefore it would have been obvious to "one of ordinary skill" in the art at the time the invention was made to use the method of having two reset discharges occur in a subfield as taught by Tokunaga et al. (US 2003/0067425) with the method taught by the combination of Awaji and Tokunaga et al. (2003/0011540) in order to provide a display device and a method of driving a display panel which are capable of improving the dark contrast.

Regarding claim 8, Awaji and Tokunaga et al. (2003/0011540) disclose a method for driving a plasma display panel, as set forth in claim 5.

Awaji and Tokunaga et al. (2003/0011540) fail to teach a method wherein a subfield reset discharge is caused to occur in order to erase the residual charges in a lit cell in the subfield immediately before the subfield in which the all-cell write discharge is caused to occur.

Tokunaga et al. (US 2003/0067425) disclose a method for driving a plasma display panel wherein a subfield reset discharge is caused to occur in order to erase the residual charges in a lit cell in the subfield immediately before another subfield (Figure 18 and paragraph [0158]. The examiner interprets that the erasure stage E is a stage in which a reset discharge is caused to occur in order to erase the residual charges in a lit cell, and that since this occurs in every cell the erasure stage would occur before the predetermined subfield.).

Therefore it would have been obvious to "one of ordinary skill" in the art at the time the invention was made to use the method of having a reset discharge in a subfield

as taught by Tokunaga et al. (US 2003/0067425) with the method taught by the combination of Awaji and Tokunaga et al. (2003/0011540) in order to provide a display device and a method of driving a display panel which are capable of improving the dark contrast.

9. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Awaji (JP 2000-148085 A) in view of Tokunaga et al. (US 2003/0067425).

Regarding claim 12, Awaji discloses a method for driving a plasma display panel, as set forth in claim 9.

Awaji fails to disclose a method wherein a subfield reset discharge is caused to occur in order to erase the residual charges in a lit cell in the subfield at the head.

Tokunaga et al. disclose a method for driving a plasma display panel wherein a subfield reset discharge is caused to occur in order to erase the residual charges in a lit cell in the subfield at the head (Figure 18 and paragraph [0158]. The examiner interprets that the erasure stage E is a stage in which a reset discharge is caused to occur in order to erase the residual charges in a lit cell, and the E stage is shown to be in the subfield at the head.).

Therefore it would have been obvious to "one of ordinary skill" in the art at the time the invention was made to use the method of having a reset discharge in a subfield at the head as taught by Tokunaga et al. (US 2003/0067425) with the method taught by the combination of Awaji and Tokunaga et al. (2003/0011540) in order to provide a

display device and a method of driving a display panel which are capable of improving the dark contrast.

10. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Awaji (JP 2000-148085 A) in view of Moon (US 2003/0098826).

Regarding claim 13, Awaji discloses a method for driving a plasma display panel, as set forth in claim 1.

Awaji fails to teach of a method wherein the widths of an address pulse and a scan pulse during the address period in the predetermined subfield are wider than those of the address pulse and the scan pulse during the address period in other subfields.

Moon discloses a method for driving a plasma display panel wherein the widths of an address pulse and a scan pulse during the address period in a subfield are wider than those of the address pulse and the scan pulse during the address period in other subfields (Paragraphs [0069]-[0071]. The examiner interprets that since the width of the scan pulses of some scan lines are larger than others and that the data pulses synchronized with the scan pulses are also set to be larger that the scan and address pulse applied during an address period would be wider than those in other subfields.).

Therefore it would have been obvious to "one of ordinary skill" in the art at the time the invention was made to use the method of having wider pulses in the predetermined subfield as taught by Moon with the method taught by Awaji in order to allow for the cells to generate high luminance.

11. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Awaji (JP 2000-148085 A) in view of Hashimoto et al. (US 2001/0017605) and further in view of Tokunaga et al. (JP 2000-276106 A).

Regarding claim 14, Awaji discloses a method for driving a plasma display panel, as set forth in claim 1.

Awaji fails to teach a method wherein the voltage of an address pulse during the address period in a subfield is raised.

Hashimoto et al. disclose a method for driving a plasma display panel wherein the voltage of an address pulse during the address period in a subfield is raised (Paragraph [0070].).

Therefore it would have been obvious to "one of ordinary skill" in the art at the time the invention was made to use the method of raising the voltage of an address pulse as taught by Hashimoto et al. with the method taught by Awaji in order to increase writing probability.

Awaji and Hashimoto et al. fail to teach a method for driving a plasma display panel wherein the voltage of a pulse in a subfield in larger than the voltage of pulses in the other subfields.

Tokunaga et al. disclose a method for driving a plasma display panel wherein the voltage of a pulse in a subfield in larger than the voltage of pulses in the other subfields (Abstract: Solution. The examiner interprets that since one subfield is indicated as to

having a pulse with a larger voltage than the other subfields, that this subfield could be the predetermined subfield.).

Therefore it would have been obvious to "one of ordinary skill" in the art at the time the invention was made to use the method of having a larger pulse voltage in the predetermined subfield as taught by Tokunaga et al. with the method taught by the combination of Awaji and Hashimoto et al. in order to enhance contrast with low power consumption while suppressing a spurious profile also and moreover to enhance display quality by stabilizing selective discharge.

12. Claims 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Awaji (JP 2000-148085 A) in view of Tokunaga et al. (JP 2000-276106 A).

Regarding claim 15, Awaji discloses a method for driving a plasma display panel, as set forth in claim 1.

Awaji fails to teach a method wherein the voltage of a scan pulse during the address period in the predetermined subfield is greater than that of the scan pulse during the address period in other subfields.

Tokunaga et al. disclose a method for driving a plasma display panel wherein the voltage of a scan pulse during the address period in the predetermined subfield is greater than that of the scan pulse during the address period in other subfields (Abstract: Solution. The examiner interprets that since one subfield is indicated as to

having a scanning pulse with a larger voltage than the other subfields, that this subfield could be the predetermined subfield.).

Therefore it would have been obvious to "one of ordinary skill" in the art at the time the invention was made to use the method of having a larger scanning voltage in the predetermined subfield as taught by Tokunaga et al. with the method taught by Awaji in order to enhance contrast with low power consumption while suppressing a spurious profile also and moreover to enhance display quality by stabilizing selective discharge.

13. Claims 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Awaji (JP 2000-148085 A) in view of Kanazawa et al. (US 2001/0054993).

Regarding claim 16, Awaji discloses a method for driving a plasma display panel, as set forth in claim 1.

Awaji fails to teach a method for driving a plasma display panel wherein a process to suppress a discharge in an unlit cell is performed between the address period and the sustain period in the predetermined subfield.

Kanazawa et al. disclose a method for driving a plasma display panel wherein a process to suppress a discharge in an unlit cell is performed between the address period and the sustain period in a subfield (Figure 17 and paragraphs [0083]-[0084].

The examiner interprets that the voltage applied to generate an auxiliary discharge is a process to suppress a discharge in an unlit cell.).

Therefore it would have been obvious to "one of ordinary skill" in the art at the time the invention was made to use the method of adding an additional pulse period as taught by Kanazawa et al. with the method for driving a plasma display panel as taught by Awaji in order to extinguish a wall charge of a cell in which an erroneous discharge has occurred.

Regarding claim 17, Awaji and Kanazawa et al. disclose a method for driving a plasma display panel, as set forth in claim 16. Kanazawa et al. also disclose wherein the process to suppress a discharge in an unlit cell is a process in which, at the same time an address pulse is applied to an address electrode (Figure 17, P1 is a pulse applied to the address electrode.), a pulse, the applied voltage of which varies as time elapses, is applied to a scan electrode (Figure 17. The pulse applied during the additional pulse period on X(X2) starts at 0V the reduces to –50V, therefore the voltage applied during the period varies as time elapses.).

Regarding claim 18, Awaji and Kanazawa et al. disclose a method for driving a plasma display panel, as set forth in claim 17. Kanazawa et al. also disclose wherein the final potential of the pulse, the applied voltage of which varies as time elapses (Figure 17, the final potential of the pulse is -50V), is lower than the finally reached potential of a charge control pulse, the applied voltage of which varies as time elapses

(Figure 17, the examiner interprets that the pulse applied to the address electrode, which starts at 0V and raises to 50 V, is the charge control pulse, in which the –50V pulse is lower than the 50V pulse.).

Conclusion

14. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Myoung et al. (US 2003/0189534) discloses of a plasma display panel driving method with an address reinforcement period between the address and sustain periods.

Nakamura (US 2003/0011542) discloses a riving method of a plasma display panel for achieving a high-quality image display by preventing an erroneous discharge.

15. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stephen G. Sherman whose telephone number is (571) 272-2941. The examiner can normally be reached on M-F, 8:00 a.m. - 4:30 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Patrick Edouard can be reached on (571) 272-7603. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

PATRICK N. EDOUARD
SUPERVISORY PATENT EXAMINER

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24 January 2006